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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/788,711	02/27/2004	Gregory E. Howard	TI-36225	6760

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EXAMINER	
VIGUSHIN, JOHN B	

ART UNIT	PAPER NUMBER
2841	

DATE MAILED: 04/04/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/788,711	HOWARD, GREGORY E.	
	Examiner	Art Unit	
	John B. Vigushin	2841	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *05 March 2004 and 07 June 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-14* is/are pending in the application.

4a) Of the above claim(s) *13 and 14* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,3,8,10 and 12* is/are rejected.

7)☒ Claim(s) *2,4-7,9 and 11* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *07 June 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Election/Restrictions

1. Restriction to one of the following inventions is required under 35 U.S.C. 121:

   I. Claims 1-12, drawn to a high frequency semiconductor device, classified in class 361, subclass 792.

   II. Claims 13-14, drawn to a method of fabricating a laminated substrate, classified in class 29, subclass 852.

The inventions are distinct, each from the other because of the following reasons:

2. Inventions I and II are related as process of making and product made. The inventions are distinct if either or both of the following can be shown: (1) that the process as claimed can be used to make another and materially different product or (2) that the product as claimed can be made by another and materially different process (MPEP § 806.05(f)). In the instant case, the product as claimed can be made by another and materially different process such as forming the traces by vapor deposition or mechanically stamping the circuit and bonding the traces on the substrate, instead of etching.

3. Because these inventions are independent or distinct for the reasons given above and have acquired a separate status in the art in view of their different classification, restriction for examination purposes as indicated is proper.

4. During a telephone conversation between Examiner Ishwar Patel and Gary Honeycutt (Reg. No. 20,250) on March 14, 2006, a provisional election was made without traverse to prosecute the invention of Group I, claims 1-12. Affirmation of this

election must be made by applicant in replying to this Office action. Claims 13-14 have been withdrawn from further consideration by the examiner, 37 CFR 1.142(b), as being drawn to a non-elected invention.

Claim Objections

5. Claim 1 is objected to under 37 CFR § 1.75(a) for the following reason:

In Claim 1, lines 4-5, "said insulator" has no antecedent basis. The objection may be overcome by changing "insulator" to –insulating substrate–.

Appropriate correction is required.

Rejections Based On Prior Art

6. The following references were relied upon for the rejections hereinbelow:

Gottlieb (US 2003/0151905 A1) Hreish et al. (US 6,661,316 B2)

Gilliland et al. (US 6,137,161)

Claim Rejections - 35 USC § 102

7. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> **A person shall be entitled to a patent unless –**
>
> **(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.**
>
> **(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States**

only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

8. Claims 1, 8, 10 and 12 are rejected under 35 U.S.C. 102(b) as being anticipated by Gilliland et al.

As to Claim 1, Gilliland et al. discloses a substrate 14 for a package 10 of high frequency semiconductor devices 12 comprising: a planar insulating substrate 14 having a plurality of parallel, planar metal layers (33, 46) embedded in the insulating substrate 14; at least one pair of parallel, metal-filled vias (parallel vias 36 or parallel vias 31) traversing substrate 14, the vias 36 and 31 having a diameter and a distance from each other of at least the diameter, and vias 36 and 31 connecting metal ports 22 and 25 on substrate 14 (Fig. 1; col.2: 28-51; col.3: 1-16); the metal in each via 36 and 31 having a sheet-like extension (flange 38) in each of selected planes of the metal layers (33, 46) (Fig. 1; col.2: 39-43; col.3: 7-11).

As to Claim 8, Gilliland et al. discloses: semiconductor chip 12 having at least a pair of bond pads 20; a planar insulating substrate 14 having a plurality of parallel, planar metal layers (33, 46) embedded in the insulating substrate 14 and input/output (I/O) ports 22 and 25 on the first (top) and second (bottom) substrate surfaces; at least one pair of parallel, metal-filled vias (parallel vias 36 or parallel vias 31) traversing substrate 14, the vias 36 and 31 having a diameter and a distance from each other of at least the diameter, and vias 36 and 31 connecting metal I/O ports 22 and 25 on substrate 14 (Fig. 1; col.2: 28-51; col.3: 1-16); the metal in each via 36 and 31 having a sheet-like extension (flange 38) in each of selected planes of the metal layers (33, 46) (Fig. 1; col.2: 39-43; col.3: 7-11); chip 12 assembled on first (top) substrate surface so

that the at least one pair of chip bond pads 20 is connected to one pair of substrate ports 22 on the first substrate surface, respectively (Fig. 1); and interconnection elements 28 attached to the second (bottom) substrate surface for connection to external parts 18 (Fig. 1; col.2: 48-59).

As to Claim 10, Gilliland et al. further discloses the connections between the pair of chip bond pads 20 and substrate ports 22 on the first substrate surface are metal bumps 24 (Fig. 1; col.2: 54-57).

As to Claim 12, Gilliland et al. further discloses the interconnection elements 28 are metal reflow bumps (Fig. 1; col.2: 57-59).

9. Claim 1 is rejected under 35 U.S.C. 102(e) as being anticipated by Gottlieb.

Gottlieb discloses, in Fig. 1, a substrate for a package of high frequency semiconductor devices comprising: a planar insulating substrate 101 having a plurality of parallel, planar metal layers $122_{1,2,3...N}$ embedded in the insulating substrate 101; at least one pair of parallel, metal-filled vias $110_{1,2}$ traversing substrate 101, the vias having a diameter and a distance from each other of at least the diameter (as can be seen in Fig. 1), the vias $110_{1,2}$ connecting the top metal portions (ports) of vias $110_{1,2}$ (that receive the semiconductor device contacts $114_{1,2}$) on substrate surface 106 and the pads $116_{1,2}$ on substrate surface 108 (Fig. 1; paragraph [0016]); and the metal in each via $110_{1,2}$ having a sheet-like extension $220_{1,2...M}$ in each of the selected planes of the metal layers $122_{1,2...N}$ (Fig. 2; paragraph [0018]; see also the second embodiment in Fig. 4, paragraphs [0024] and [0025], wherein each of the vias have sheet-like extensions in plural metal layers).

Claim Rejections - 35 USC § 103

10. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

11. Claim 3 is rejected under 35 U.S.C. 103(a) as being unpatentable over Gilliland et al. in view of Hreish et al.

I. Gilliland et al. discloses the metal extensions 38 form capacitances with ground layers 33 in the low pass filter of Figs. 1 and 2, and that the metal extensions 38 are attached to the via metal 36 (col.3: 7-11 and 44-61) but does not teach the shape of the metal extensions 38.

II. Hreish et al. discloses metal extensions (59 in Fig. 6 and 59A,B in Fig. 17) that are attached to the metal of a via 56 and form capacitances with the other layers 58 of the circuit board as part of a low pass filter (Figs. 6, 7 and Figs. 17, 18), the metal extensions 59 (Fig. 6) and 59A,B (Fig. 17) shaped approximately as rings which surround the via in the plane of each metal layer 58 within which they are formed (col.4: 11-17 and 36-41; col.9: 20-32).

III. Since Gilliland et al. and Hreish et al. are both from the same field of high frequency circuit boards with built-in low pass filters, the annular (ring) shape of the metal extensions for forming the capacitance components of the low pass filter, as

disclosed by Hreish et al., would have been recognized in the pertinent art of Gilliland et al.

IV. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to shape the metal extensions of Gilliland et al. as rings in order to form the capacitance components of the built-in low pass filter, as taught by Hreish et al.

12. Claims 8, 10 and 12 are rejected under 35 U.S.C. 103(a) as being unpatentable over Gottlieb in view of Gilliland et al.

A) As to Claim 8:

I. Gottlieb discloses, in Fig. 1: a semiconductor chip 102 having at least one pair of bond pads (corresponding to connector means $114_{1,2}$); a planar insulating substrate 101 having a plurality of parallel, planar metal layers $122_{1,2,3...N}$ embedded in the insulating substrate 101 and input/output (I/O) ports (top portions of vias $110_{1,2}$) and pads $116_{1,2}$ on the first (top) and second (bottom) substrate surfaces; at least one pair of parallel, metal-filled vias $110_{1,2}$ traversing substrate 101, the vias having a diameter and a distance from each other of at least the diameter (as can be seen in Fig. 1), the vias $110_{1,2}$ connecting the top metal portions (ports) of vias $110_{1,2}$ (that receive the semiconductor device contacts $114_{1,2}$) on substrate surface 106 and the pads $116_{1,2}$ on substrate surface 108 (Fig. 1; paragraph [0016]); and the metal in each via $110_{1,2}$ having a sheet-like extension $220_{1,2...M}$ in each of the selected planes of the metal layers $122_{1,2...N}$ (Fig. 2; paragraph [0018]; see also the second embodiment in Fig. 4, paragraphs [0024] and [0025], wherein each of the vias have sheet-like extensions in

plural metal layers); chip 102 assembled on the first (top) substrate surface so that the at least one pair of chip bond pads is connected to one pair of the substrate ports on the first (top) substrate surface, respectively (Fig. 1).

II. Gottlieb discloses connection of ports 1161,2 to external parts 104 but does not indicate the interconnection elements attached to the ports for that purpose. Gottlieb does, however, teach that the external parts 104, as well as the electronic components 102, may be passive devices and active devices, which include integrated circuit semiconductor chips, such as that of electronic component 102 (paragraph [0016]).

III. Gilliland et al. discloses interconnection elements 28 (solder balls) attached to the ports 25 on the bottom surface of a multilayer substrate for connection to external parts 18.

IV. Since both Gottlieb and Gilliland et al. are both in the same art of multilayer circuit boards for carrying signals of a chip on a top surface port to an external part connected to a bottom surface port, then the use of solder ball interconnection elements attached to the ports on the second surface for connection to an external part structured to receive the solder ball interconnection elements, as taught by Gilliland et al., would have been readily recognized in the pertinent art of Gottlieb, wherein it is taught that the external part may be an integrated circuit semiconductor chip with bond pads just like the chip connected to the top surface port.

V. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to employ interconnection elements, such as solder balls, attached to the ports $116_{1,2}$ on the second substrate surface of Gilliland et al. for

connection to an external part that is configured with pads that receive solder balls, as taught by Gilliland et al., wherein the electronic component 104 of Gottlieb is a semiconductor integrated circuit like component 102, as taught by Gottlieb.

B) As to Claim 10, modified Gottlieb further discloses the connections between the pair of chip bond pads and the substrate ports on the first (top) substrate surface are metal bumps $114_{1,2}$.

C) As to Claim 12, it has already been established in the rejection of Claim 8, above, over Gottlieb in view of Gilliland et al., that the interconnection elements attached to the ports $116_{1,2}$ on the second (bottom) substrate surface for connection to the external parts 104, when the external parts 104 are semiconductor chips like chip 102 on the first (top) substrate surface, of modified Gottlieb, are metal (solder) reflow bumps.

Allowable Subject Matter

13. Claims 2, 4-7, 9 and 11 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

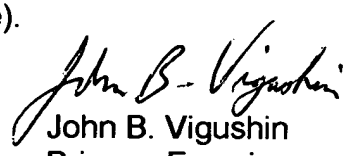
14. As allowable subject matter has been indicated, applicant's reply must either comply with all formal requirements or specifically traverse each requirement not complied with. See 37 CFR 1.111(b) and MPEP § 707.07(a).

Conclusion

15. Any inquiry concerning this communication or earlier communications from the examiner should be directed to John B. Vigushin whose telephone number is 571-272-1936. The examiner can normally be reached on 8:30AM-5:00PM Mo-Fri.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kamand Cuneo can be reached on 571-272-1957. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).



John B. Vigushin
Primary Examiner
Art Unit 2841

jbv
March 29, 2006